Implementing ISO 15288 V&V Processes using the V&V Studio

(Smart way to increase V&V digitalization)

THE REUSE COMPANY

January, 2021

Presenters' List

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Presentation

Systems Engineering Context

Verification Vs Validation

What to Verify / Validate

How to Verify / Validate

Verification / Validation Techniques

ISO Verification Process Description

Digitalizing the Verification Process

Introduction to The REUSE Company

01 The company was created in **1999**

As a spin-off of a University in Europe

02 **System + Software Engineers**

Smart combination between Company staff and R&D from Academia

03 **Headquarters:**
Madrid (Spain)

International offices:
Stockholm (Sweden)
Tokyo (Japan) Delegation

2021:
USA
Chicago/Detroit/Miami

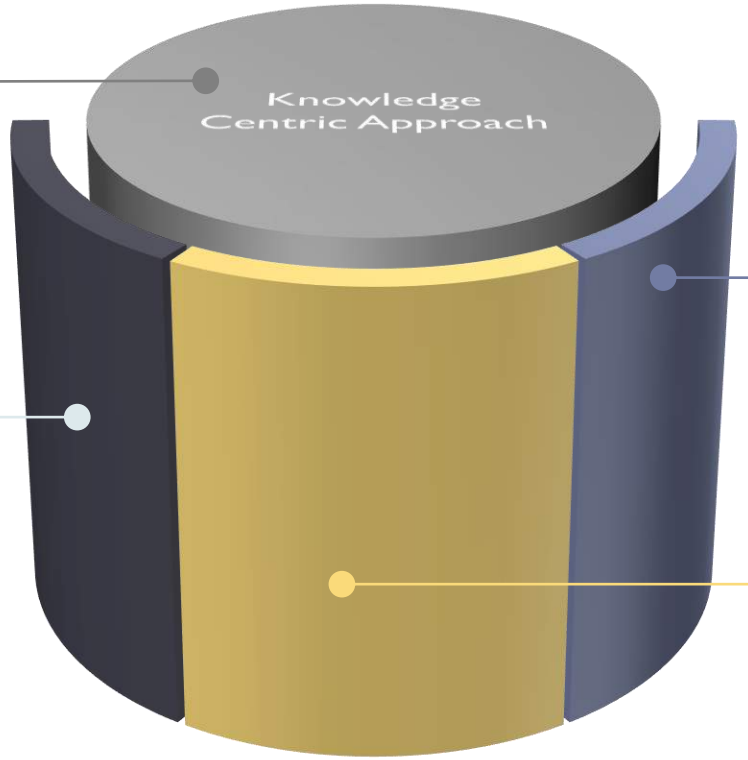
04 To promote a **reusable**, **scalable** and global solution to a **smart** and **interoperable** Systems Engineering environment, by offering a **semantic knowledge centric** approach.

the REUSE company

T(he) R(euse) Q(ompany)

Knowledge Centric Systems Engineering (KCSE)

Global Repositories –
Archiving –
Configuration Management –



TRACEABILITY

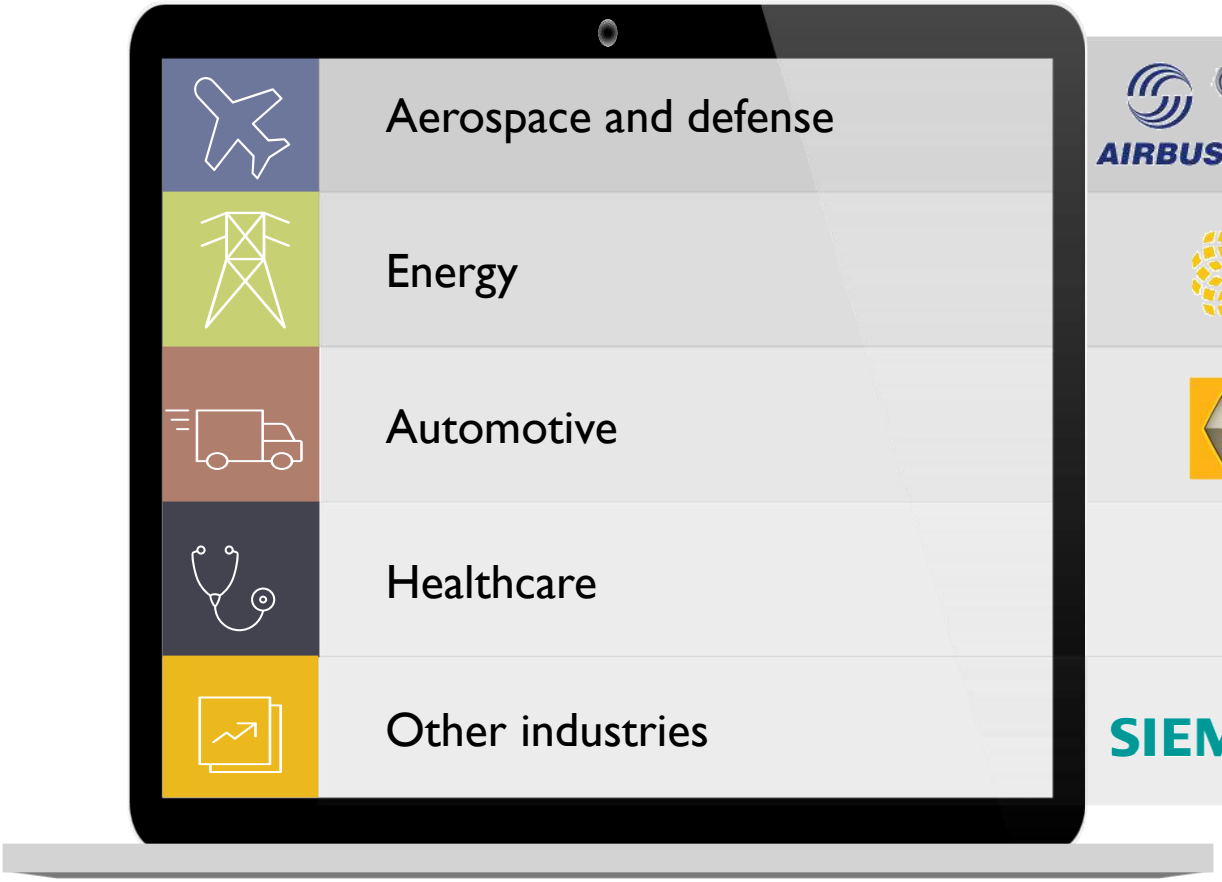
Links and Interoperability –
Transformations –
Change management –

QUALITY (ies)

- Quality Management
- Verification & Validation management
- Risks Management
- Smart Authoring

REUSABILITY

- Interoperability
- Retrieval & Archiving
- Adaptability to Existing Toolsets



AIRBUS
AIRBUS DEFENCE & SPACE
AIRBUS GROUP INNOVATIONS
SAFRAN AIRCRAFT ENGINES
THALES
HENSOLDT
THALES Communications & Security S.A.S.
aes
arianeGROUP
FUSION FOR ENERGY
iter the way to new energy
EDF
REPSOL
RENAULT
Ford
FCA FIAT CHRYSLER AUTOMOBILES
TOYOTA
THINK SURGICAL
Health Net
SIEMENS
acciona Agua
orange
rtve
ELRA European Land Registry Association
tirant lo blanch

José Manuel Pereira BIO

- Member of the Tec4Com department in TRC.
- Responsible for the Temperature War SE Use Case.

- Systems Engineering Methodology thesis development.
- Complete SE Use Case based on the INCOSE 15288 Standard.
- Supervised training under the former president of INCOSE Spain.
- Degree in Computer Science and Engineering.

José M. Pereira
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Page Layout explanation

⇦ Describes content coming from the Systems Engineering Handbook or the ISO15288 Standard

Describes content coming from the "Practical Way to implement ISO 15288 V&V processes (using The REUSE Company's V&V Studio ⇨

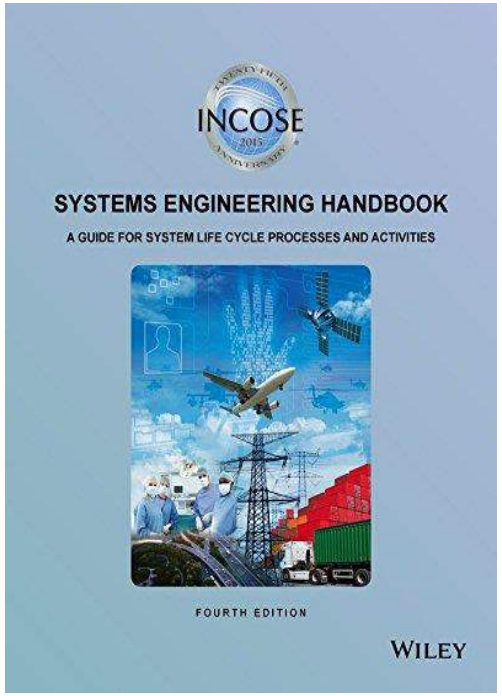
⇦ Extends content for V&V Processes inside the Systems Engineering Handbook

⇦ Extends content by describing how the concept is implemented in the V&V Studio Software tool

⇦ Pointer to the table of contents

Describes content used in the V&V Studio Software tool ⇨

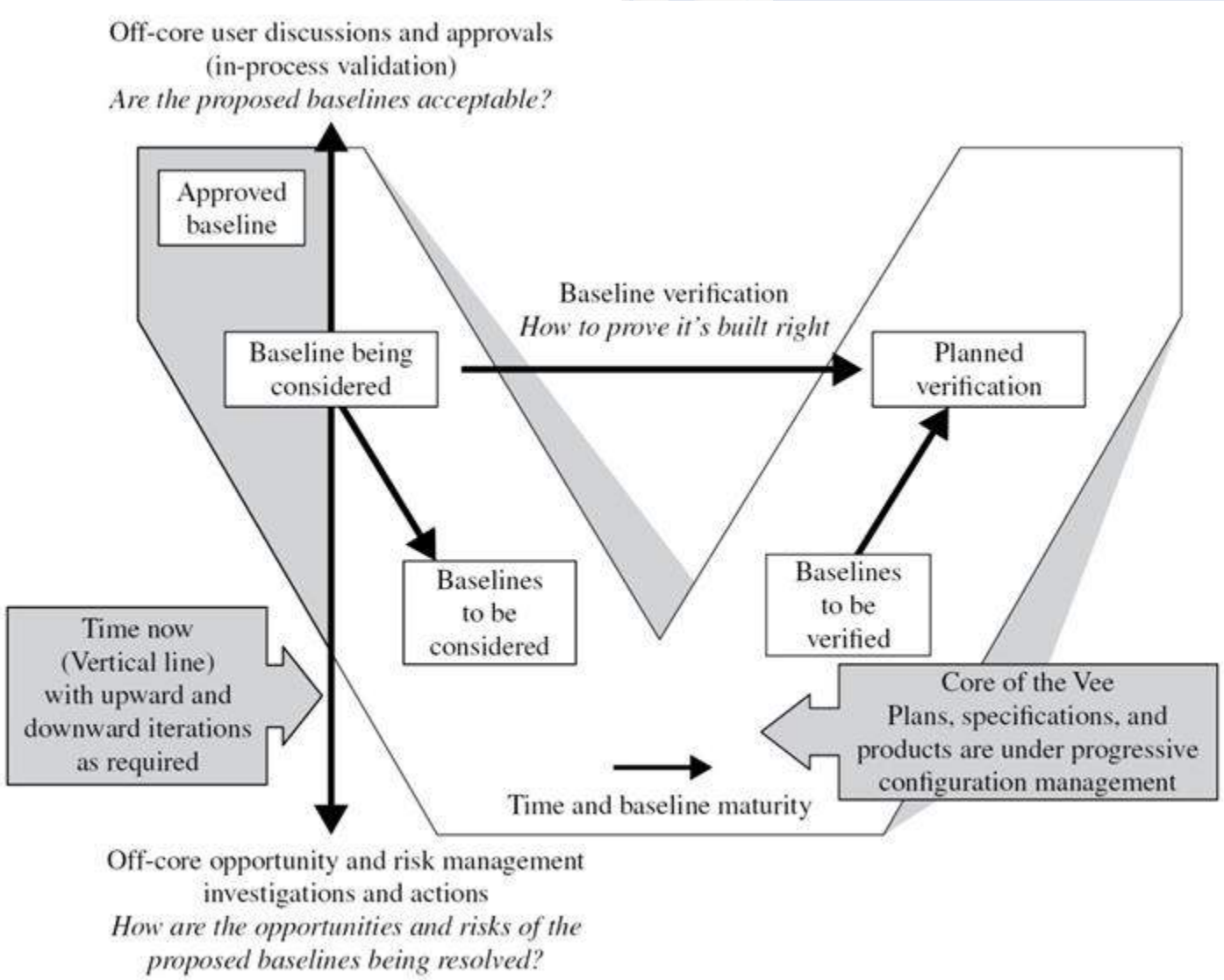
V&V (Verification and Validation) Processes within the ISO 15288 – Systems Engineering Standard



KEY CONCEPTS : Development Life-Cycle - V (VEE) MODEL

- The core of the Vee (i.e., those products that have been placed under configuration control) depicts the evolving baseline from stakeholder requirements agreement to identification of a system concept to definition of elements that will comprise the final system.

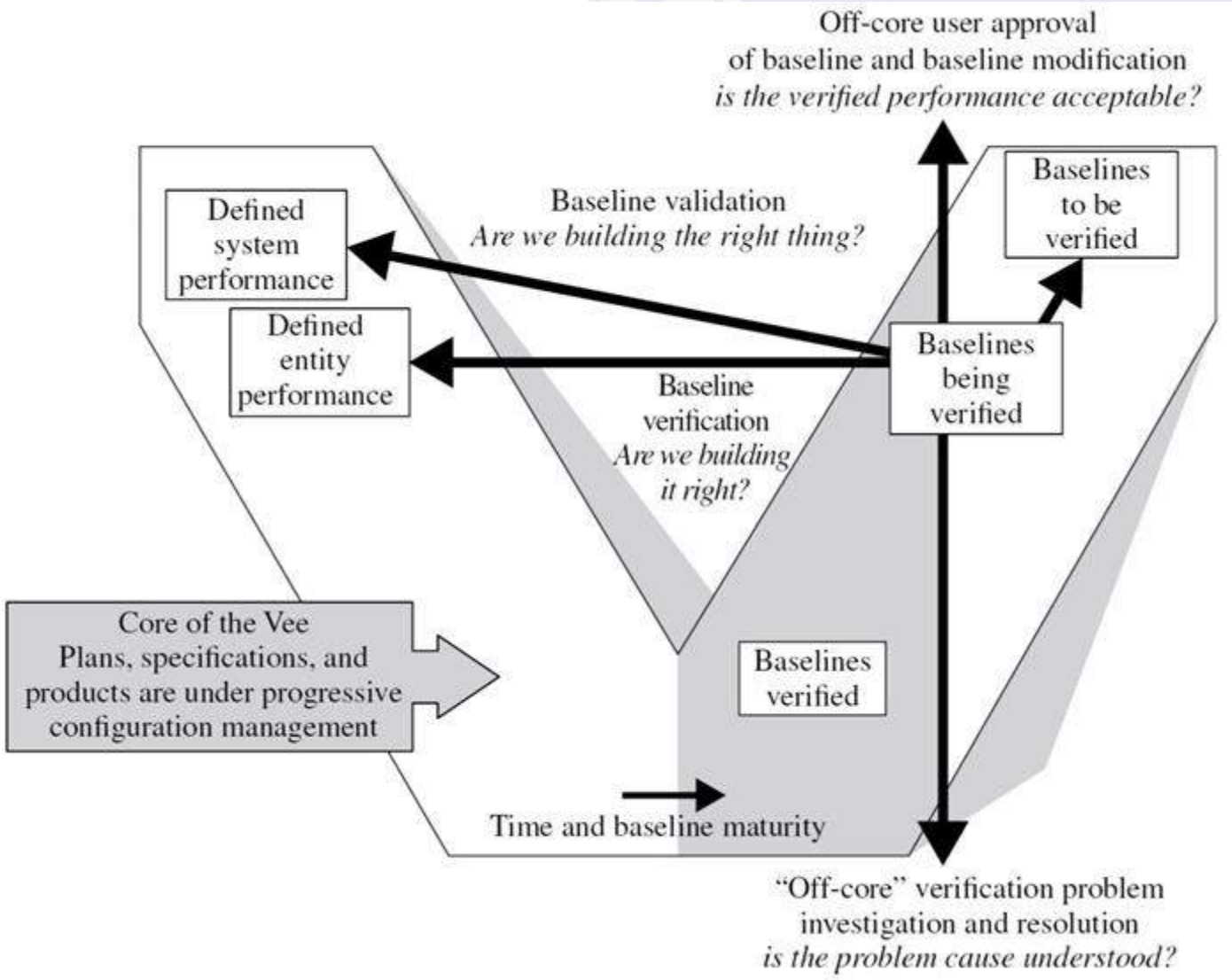
- With time moving to the right, the evolving baseline defines the left side of the core of the Vee, as shown in the shaded portion of Figure



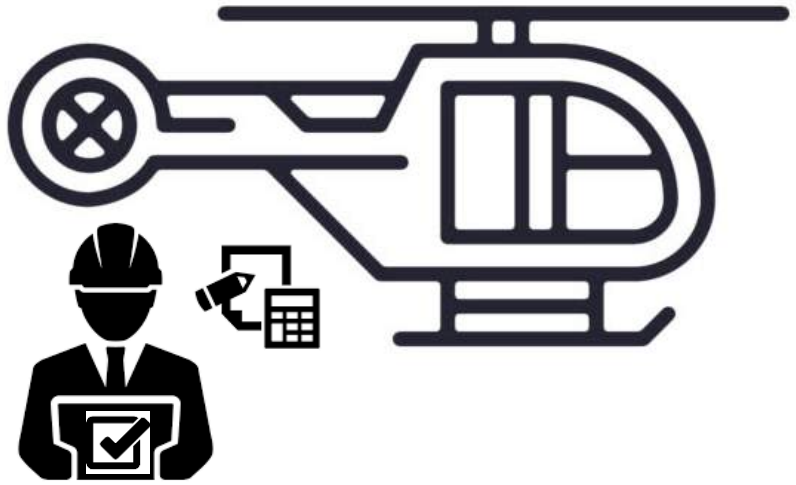
V-Model - Forsberg et al. (2005)

KEY CONCEPTS : Development Life-Cycle - V (VEE) MODEL

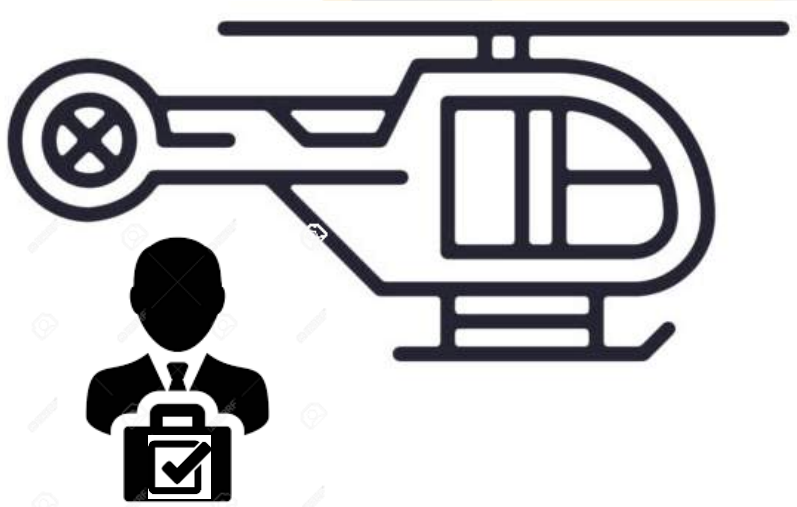
- As entities are implemented, verified, and integrated, the right side of the core of the Vee is executed.
- Since one can never go backward in time, all iterations in the Vee are performed on the vertical "time now" line.
- Upward iterations involve the stakeholders and are the in-process validation activities that ensure that the proposed baselines are acceptable.
- The downward vertical iterations are the essential off-core opportunity and risk management investigations and actions.
- In each stage of the system life cycle, the SE processes iterate to ensure that a concept or design is feasible and that the stakeholders remain supportive of the solution as it evolves.



V-Model - Forsberg et al. (2005)



Verification



Validation

Verification Process (ISO/IEC/IEEE 15288)

- "*The purpose of the Verification process is to provide objective evidence that a system or system element fulfills its specified requirements and characteristics.*" (SEHb p.83)
  - The purpose of the verification process is to provide evidence that no error/defect/fault has been introduced at the time of any transformation of inputs into outputs; it is used to confirm that this transformation has been made "right" according to the requirements and selected methods, techniques, standards, or rules.

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Verification and Validation are not the same

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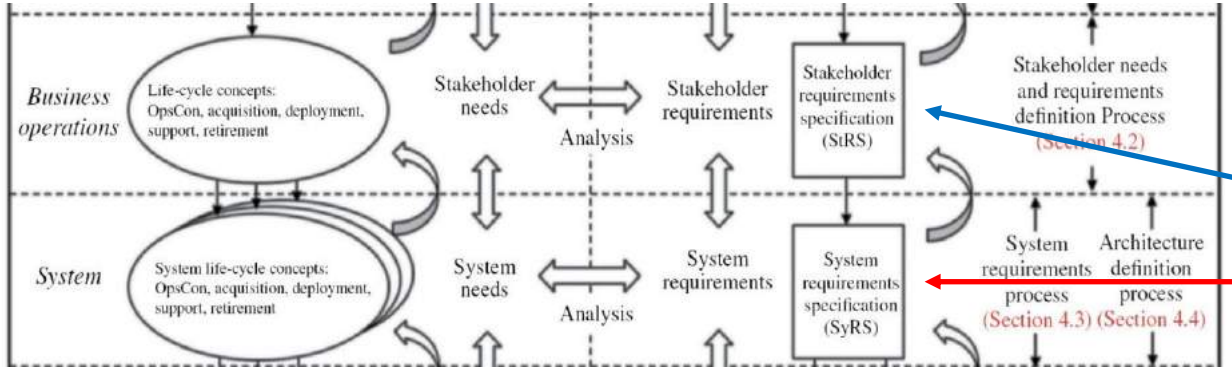
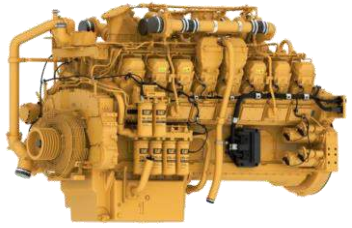


Source: Mike Ryan - > SE Handbook V4

Validation

Verification



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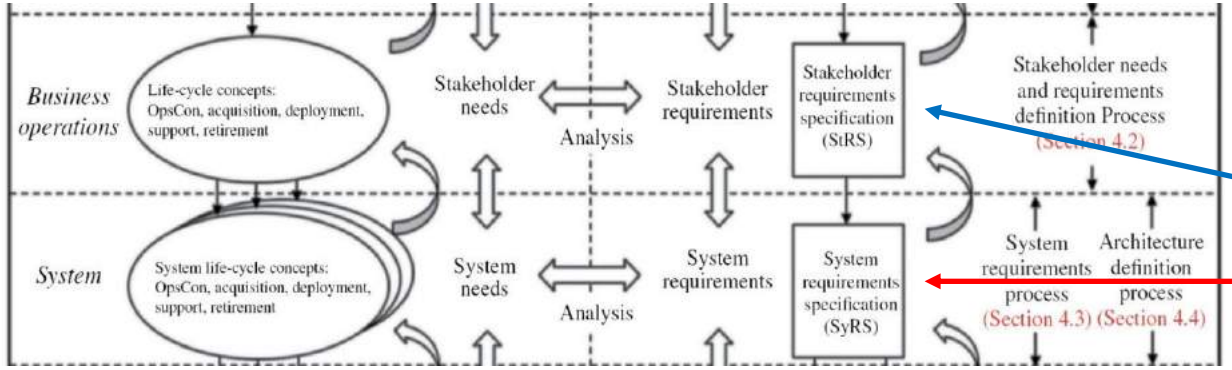

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Validation

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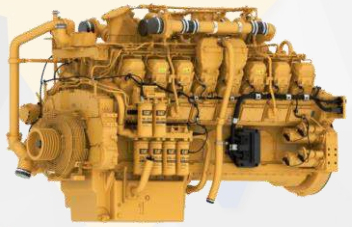
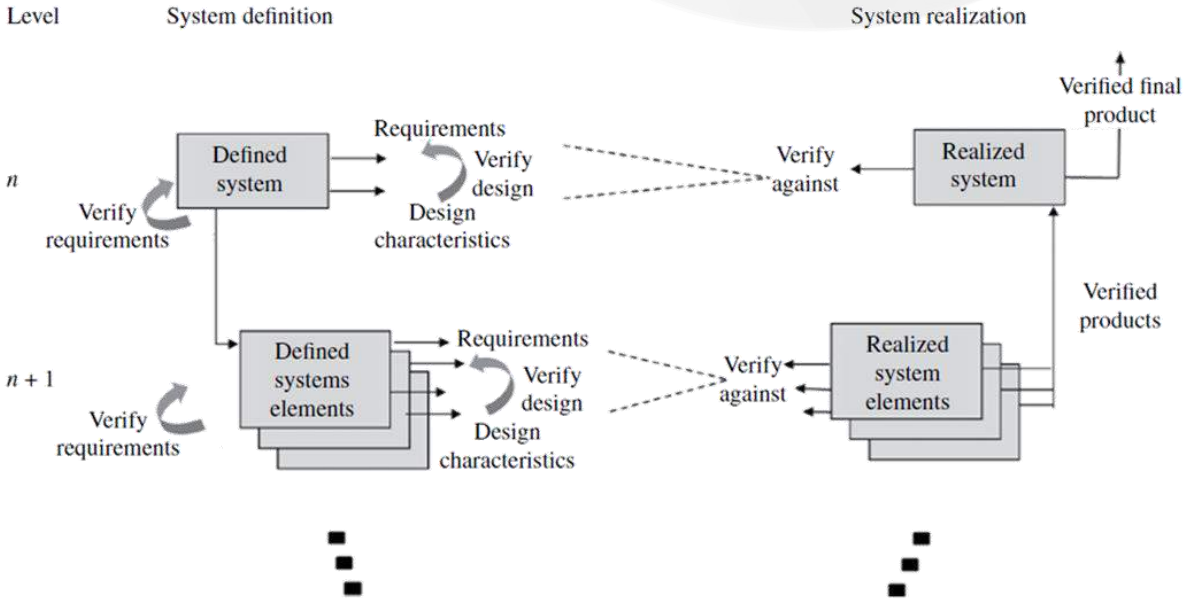


- Verification and Validation are not the same (*"build the thing right"* vs *"build the right thing"*):
  - Context is (very) different
  - Scope is different
  - … even if both use the same methods and tools
- But, the digitalization of both can be based on the same methods and activities (we´ll see them ASAP)
  - Therefore, we'll offer the same tool (with different sections) to manage both Verification and Validation

What to Verify / Validate

What to Verify / Validate

- The INCOSE Systems Engineering handbook (V4) states the focus in a more precise way:
  - *"The verification process can be applied to any engineering element that has contributed to the definition and realization of the system itself (e.g., verification of a system requirement, a function, an input/output flow, a system element, an interface, a design property, a verification procedure)".* (SEHb p.83)
- This statement widens the Verification process goal to what it really stands for:
  - To provide objective evidence that whatever engineering item (requirement, requirements set, model element, model(s), function, etc.), system element or the SOI itself has been "built right".
- The result is that the Verification process must be applied universally and transversely both R2L of the V-Model (the most known) as well as L2L (or even R2R)



Source: Systems Engineering Handbook V4 - Fig 4.15 p.87

What to verify controversy

Verify the Requirements against the SOI / SE?

Verify the SOI / SE against the Requirements?

Items	Explanation for Verification
Document	To verify a document is to check the application of drafting rules.
Stakeholder Requirement and System Requirement	To verify a stakeholder requirement or a system requirement is to check the application of syntactic and grammatical rules, characteristics defined in the stakeholder requirements definition process, and the system requirements definition process such as necessity, implementation free, unambiguous, consistent, complete, singular, feasible, traceable, and verifiable.
Design	To verify the design of a system is to check its logical and physical architecture elements against the characteristics of the outcomes of the design processes.
System	To verify a system (product, service, or enterprise) is to check its realized characteristics or properties against its expected design characteristics.
Aggregate	To verify an aggregate for integration is to check every interface and interaction between implemented elements.
Verification Procedure	To verify a verification procedure is to check the application of a predefined template and drafting rules.

https://www.sebokwiki.org/wiki/System_Verification

Items	Explanation for Verification
Architecture of the System	To check the correct application of patterns and heuristics & correct usage of modeling techniques or methods.
Design of a System Element	To check the correct usage of patterns, trade rules, or state of the art related to the concerned technology. Verification of a system (product, service, or enterprise) or system element
System	To check its realized characteristics or properties (e.g., as measured) against its specified requirements, expected architectural characteristics, and design properties (as described in the requirements, architecture, and design documents)

SE Handbook V4 – p 85.

Why the debate? -> For Tool Vendor to decide meta-model

What to verify controversy

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SE Handbook V4 – p 85.

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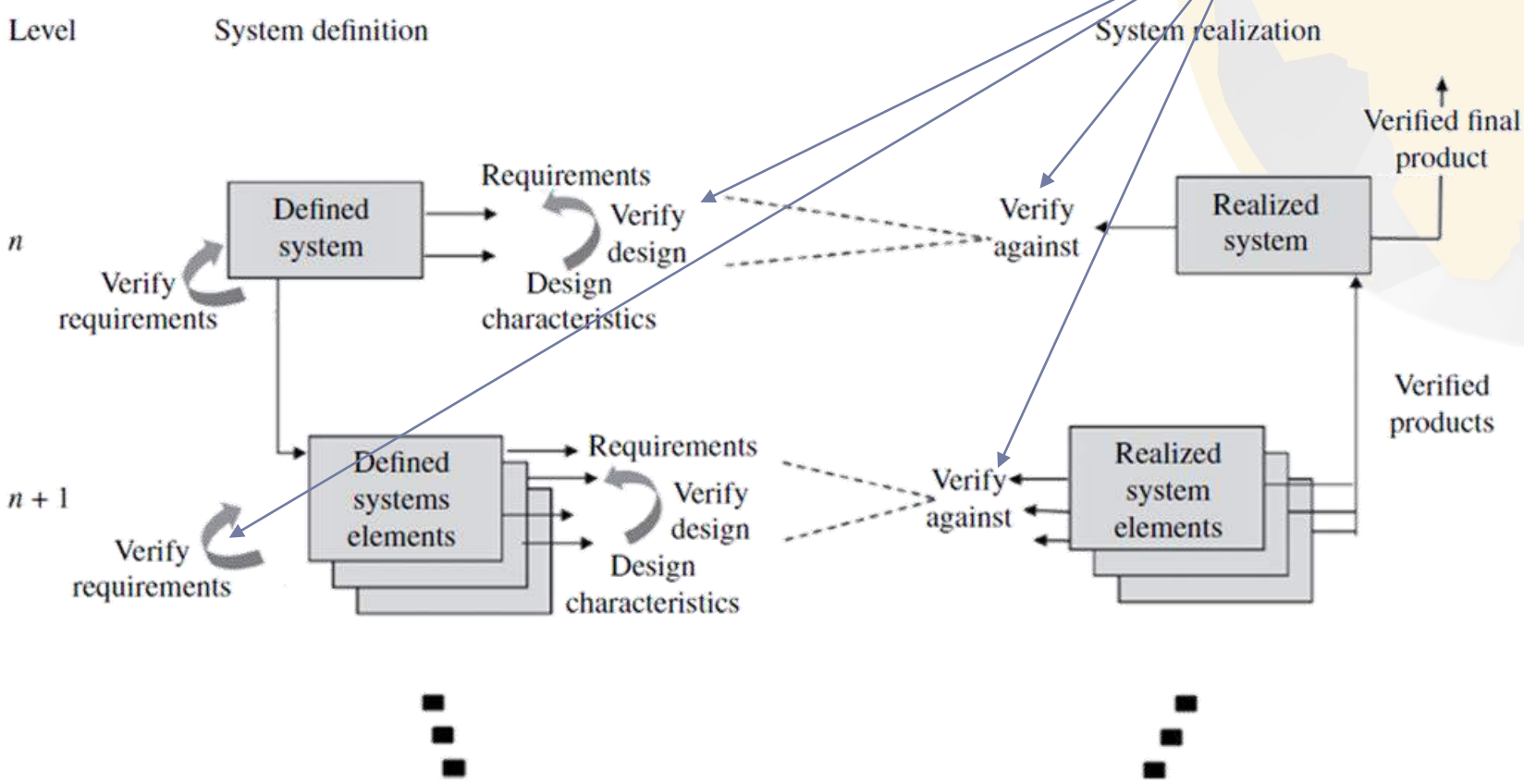


Source: Systems Engineering Handbook V4 - Fig 4.15 p.87

What to verify controversy

Verify the Requirements against the SOI / SE?

Verify the SOI / SE against the Requirements?

4.9.2.1 Notion of Verification Action A verification action describes what must be verified (e.g., a requirement, a characteristic, or a property as reference), on which item (e.g., requirement, function, interface, system element, system), the expected result (deduced from the reference), the verification technique to apply (e.g., inspection, analysis, demonstration, test), and on which level of decomposition of the system (e.g., SOI, intermediate level system element, leaf level system element).

Source: SEH V4 - p.85

4.3.2.2 Characteristics and Attributes of Good Requirements In defining requirements, care should

… Source: SEH V4 - p.60

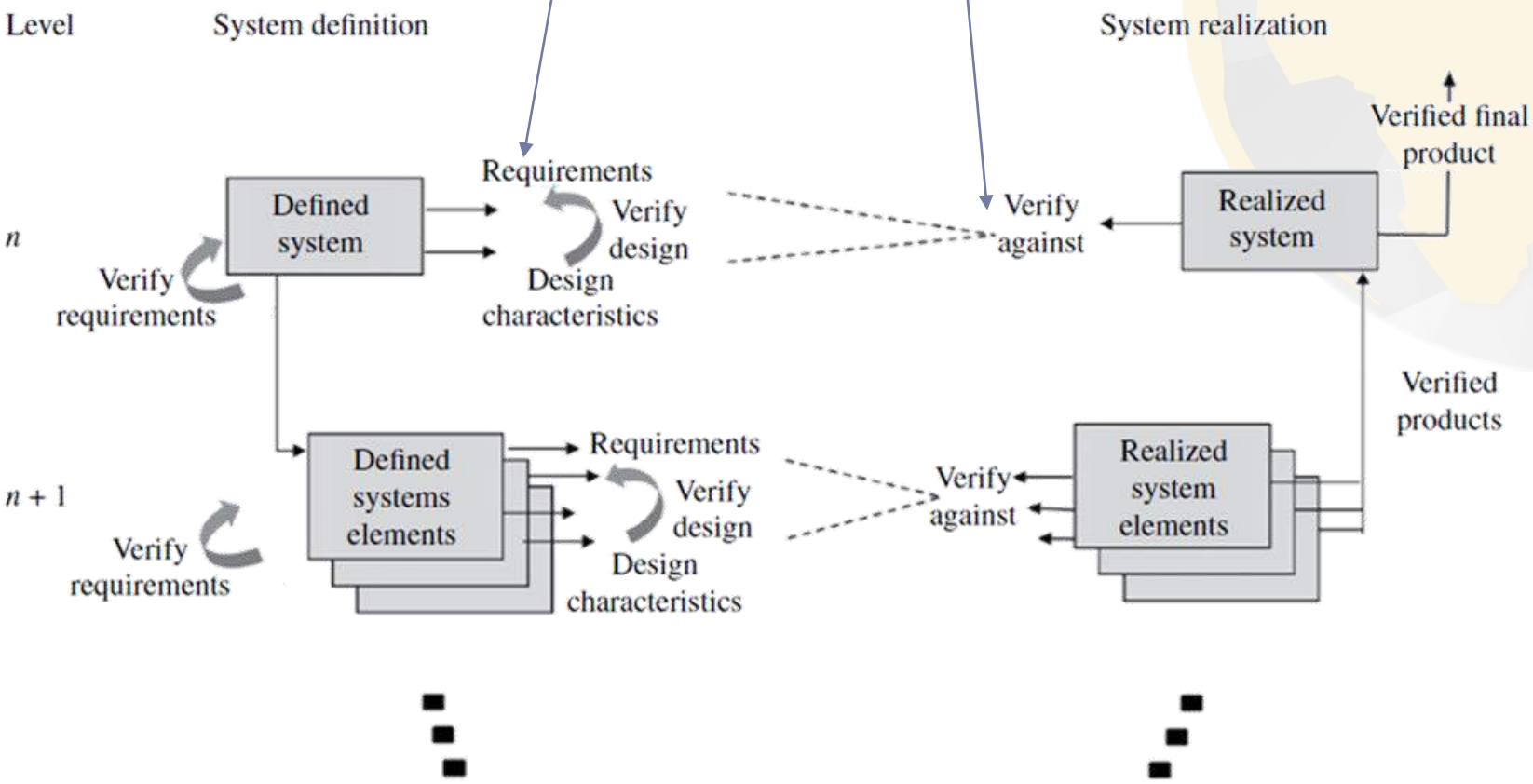
- *Verifiable*—Each requirement must be verified at some level by one of the four standard methods (inspection, analysis, demonstration, or test). A customer may specify, "The range shall be as long as possible." This is a valid but unverifiable requirement. This type of requirement is a signal that a trade study is needed to establish a verifiable maximum range requirement. Each verification requirement should be verifiable by a single method.

Source: SEH V4 - p.61

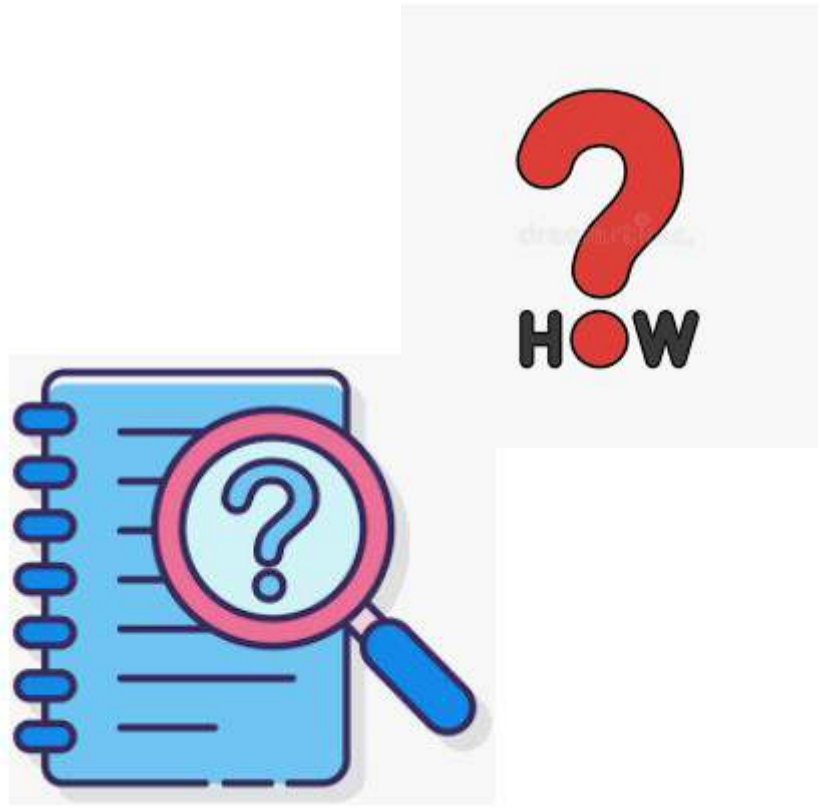
What to verify controversy

Verify the verifiable item against Source Items

You decide your way ☺

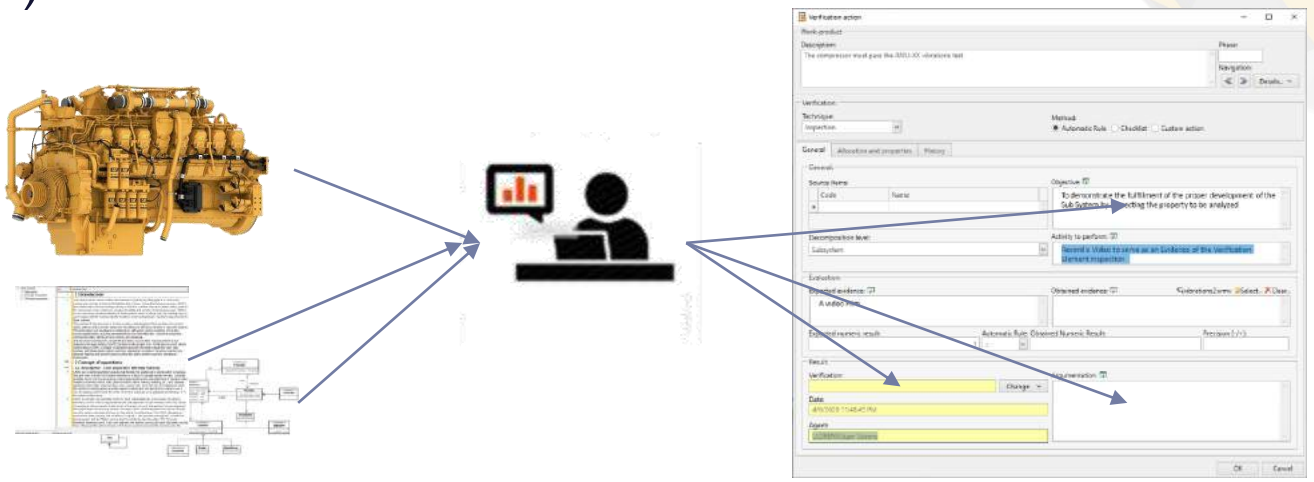


Source: Systems Engineering Handbook V4 - Fig 4.15 p.87



How to Verify / Validate

- The Verification Process implementation evolves around the notion of VERIFICATION ACTION.
- A Verification Action defines a structured representation (digital) of the necessary information used to assure that the verified element fulfills its specified requirements and characteristics.
- The Verification Action (VA) is intended to serve as a mean to provide objective evidence that a work-product has (or has not) been verified.



- The process of defining, configuring, scheduling, filling, analyzing, managing and reporting VAs is called the Verification Process

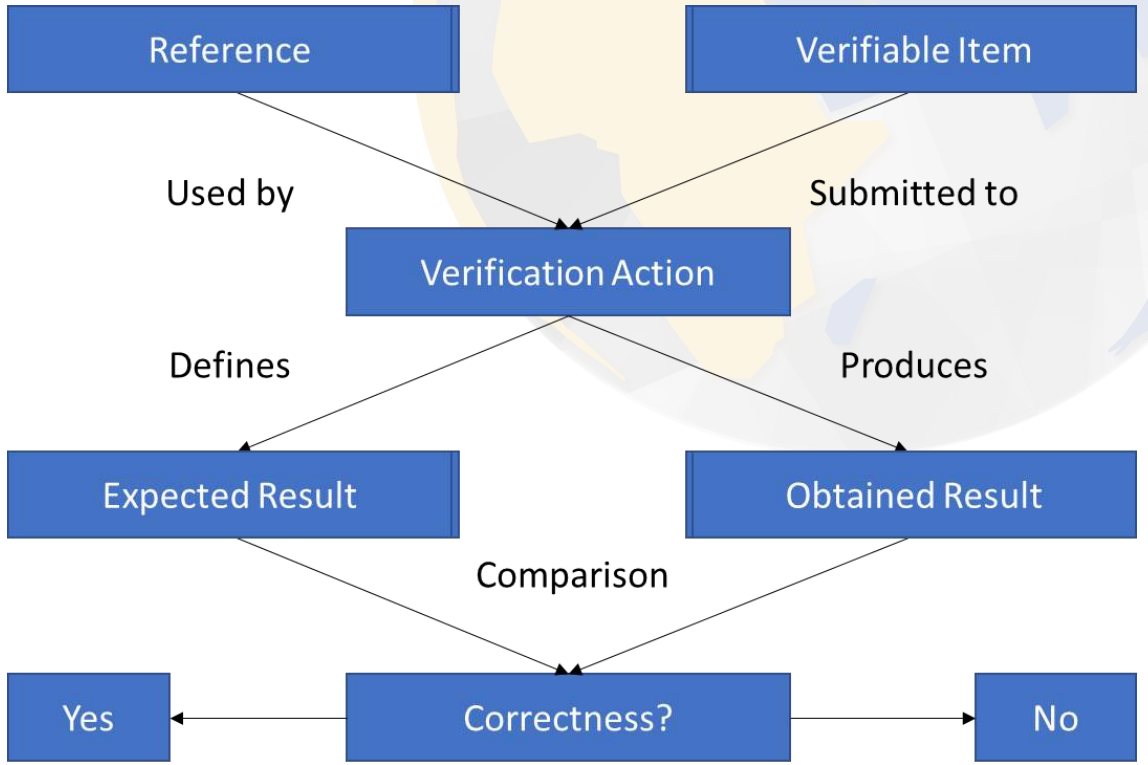
VERIFICATION PROCESS: ELABORATION

- Notion of Verification Action:

  - A verification action describes WHAT MUST BE VERIFIED (e.g., a requirement, a characteristic, or a property as reference, the system), ON WHICH ITEM (e.g., requirement, function, interface, system element, system), the expected result (deduced from the reference), the verification technique to apply (e.g., inspection, analysis, demonstration, test), and on which level of decomposition of the system
  - The performance of a verification action onto the submitted item provides an obtained result which is compared with the expected result.

How does it work in V&V Studio

- The process of verifying a work-product is simply to compare predefined information (a reference) with real information and confirm that the comparison produces the expected results
  - The information for comparing results and other administrative data must be stored in a Verification Action
  - A VA is considered passed when the obtained result fulfills the defined criteria of comparison with the expected result, producing an evidence
  - Attributes of the Verification Action 



- The V&V Studio is capable to launch the verification process automatically (comparison operation)
  - The comparison process allows the computer to assign a state to the VA

Automatic Verification Process

Predefine the Reference Information in a VA Technique, Method, resources, etc)

Connect to the Verifiable information supporting Tool (DOORS, Excel, TeamCenter, etc.) and assign a VA to each one of them

Reference

Verifiable Item

Used by

Submitted to

Verification Action

Defines

Produces

Predefine what value must be expected

Obtain the Verification results (Automatically or manually)

Expected Result

Obtained Result

Comparison

Computer Assigns "Suggested YES" State to VA

Yes

Correctness?

No

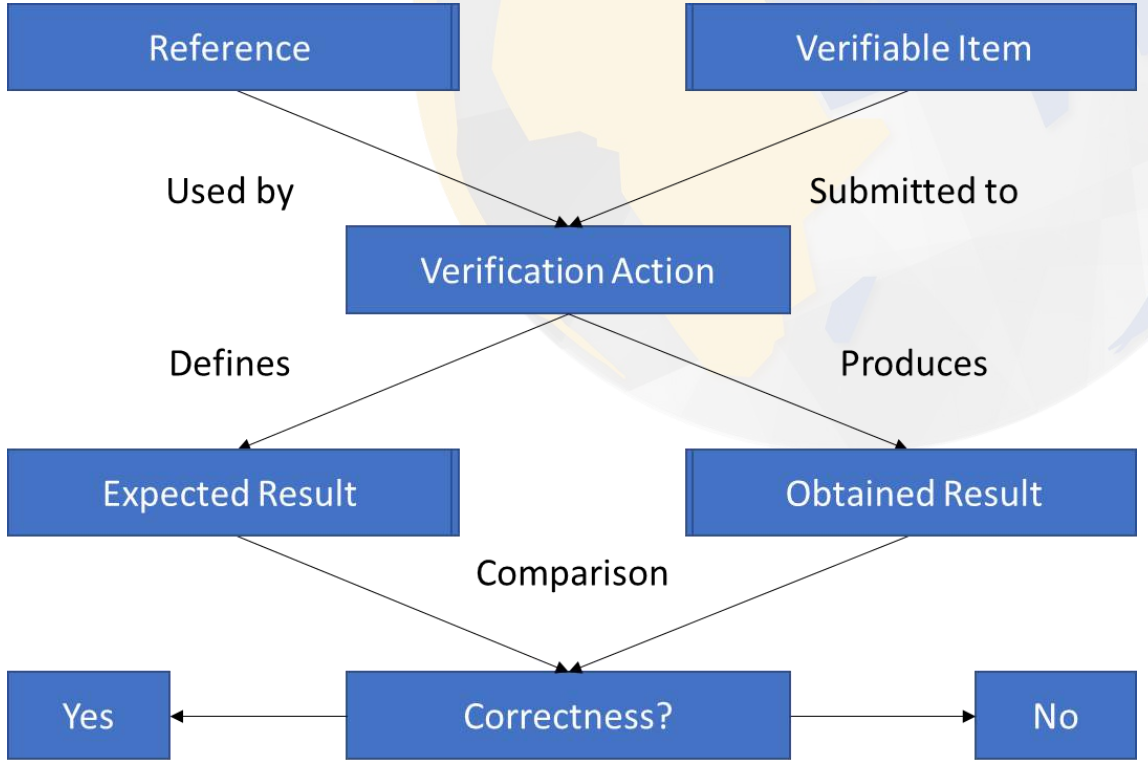
Computer Assigns "Suggested NO" State to VA

Engineer decides Final value

A quality comparison function is automatically calculated

Engineer decides Final value

- Relevant Concepts:
  - Expected Result
  - Obtained Result
    - Different methods for obtaining results
  - The Comparison Operation
  - The Verification Action STATE



V&V Studio Methods for OBTAINING Results

COMPARISON operations in the V&V Studio

STATES of the Verification Action

VERIFICATION PROCESS: ELABORATION

- Verification Level per Level:
  - Every system and system element are verified, and any findings possibly corrected before being integrated into the system of the higher level.
  - As necessary, systems and system elements are partially integrated in subsets (aggregates) in order to limit the number of properties to be verified within a single step.

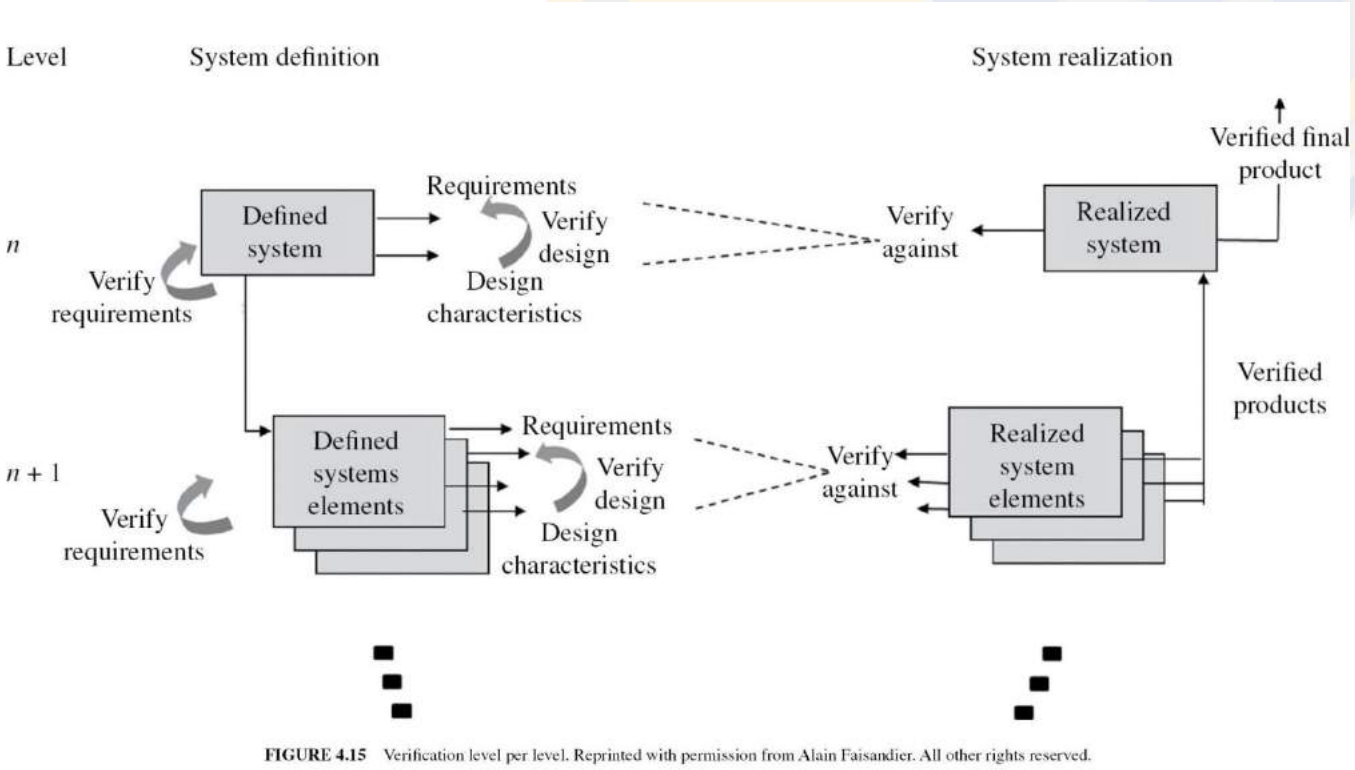


FIGURE 4.15 Verification level per level. Reprinted with permission from Alain Faisandier. All other rights reserved.

Source: Handbook

Verification and Validation Techniques

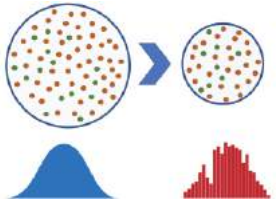
Inspection

Demonstration

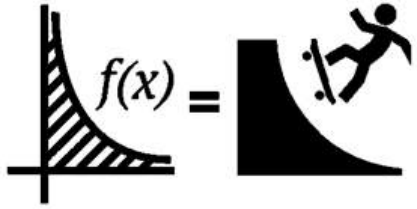
Test

Analogy or Similarity

Sampling



Analysis / Simulation



Inspection Verification technique

Inspection

- Based on visual or dimensional examination of an element
- Relies on the human senses
  - or uses simple methods of measurement and handling.
- Generally nondestructive
  - and typically includes the use of sight, hearing, smell, touch, and taste
- Simple physical manipulation / mechanical and electrical gauging / and measurement.
- No stimuli (tests) are necessary

How to define an Inspection VA in the V&V Studio

Demonstration Verification technique

Demonstration

- Used to show correct operation of the submitted element against operational and observable characteristics without using physical measurements
  - (or minimal instrumentation or test equipment).
- Generally uses a set of actions, selected to show that the element response to stimuli is suitable
  - or to show that operators can perform their assigned tasks when using the element.
- Observations are made and compared with predetermined/expected responses

How to define a Demonstration VA in the V&V Studio

Test

- Performed onto the submitted element by which functional, measurable characteristics, operability, supportability or performance capability is quantitatively verified when subjected to controlled conditions that are real or simulated.
- Often uses special test equipment or instrumentation to obtain accurate quantitative data to be analyzed.

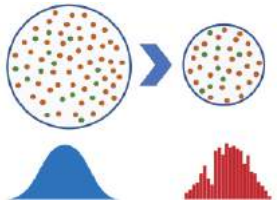
How to define a Test VA in the V&V Studio

Analogy / Similarity Verification technique

Analogy or Similarity

- Based on evidence of similar elements to the submitted element or on experience feedback.
  - It is absolutely necessary to show by prediction that
    - the context is invariant
    - the outcomes are transposable.
    - (e.g., models, investigations, experience feedback).
- Can only be used if the submitted element is similar in design, manufacture, and use.
- Equivalent or more stringent verification actions were used for the similar element.
- The intended operational environment is identical to or less rigorous than the one applied to the similar element.
- Often considered as a type of analysis technique.

How to define an Analogy VA in the V&V Studio

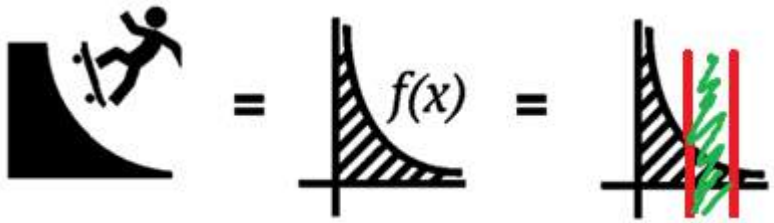


Sampling

- Based on verification of characteristics using samples.
- The number, tolerance, and other characteristics must be specified and in agreement with the experience feedback.

How to define a Sampling VA in the V&V Studio

Analysis Verification technique

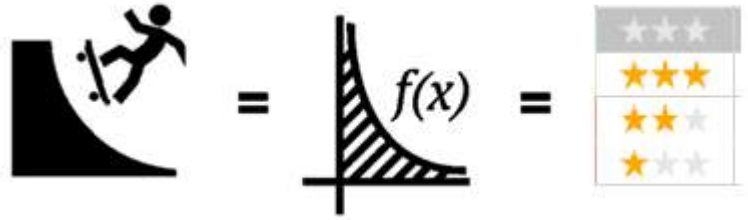


Analysis / Simulation

- Based on analytical evidence
  - obtained without any intervention on the verifiable element.
- To show theoretical compliance => Mathematical or probabilistic calculation, logical reasoning (including the theory of predicates), modelling and/or simulation under defined conditions.
- Mainly used where testing to realistic conditions cannot be achieved or is not cost-effective.

How to define an Analysis/Simulation VA in the V&V Studio

Analysis Verification technique



Specific Analysis: Quality Analysis

- Based on analytical evidence about the quality of the Verifiable Item (Using RQA from The REUSE company)
  - Obtained without any intervention on the verifiable element.
- To show theoretical compliance => Mathematical or probabilistic calculation, logical reasoning (including the theory of predicates), modelling and/or simulation under defined conditions.
  - Compare expected quality with obtained quality
- Used when quality judgement exists.

How to define a Quality Analysis VA in the V&V Studio

Verification Technique \ Verification Method	*Manual Insertion of numeric values*	*Check List*	*Custom Verification*	*Quality calculation*
Inspection	X	X	X	
Analysis	X	X	X	
Quality Analysis	X	X	X	
Demonstration	X	X	X	
Test	X	X	X	
Analogy or Similarity	X	X	X	
Sampling	X	X	X	
V&V Studio Quality Analysis			X	X
Other	X	X	X	

ISO 15288 – Verification Process

Controls

Inputs
- Life cycle concepts
- System requirements
- Verification criteria
- Updated RVTM
- Interface definition
- Integrated system or system elements
- Integration report

Activities
- Prepare for verification
- Perform verification
- Manage results of verification

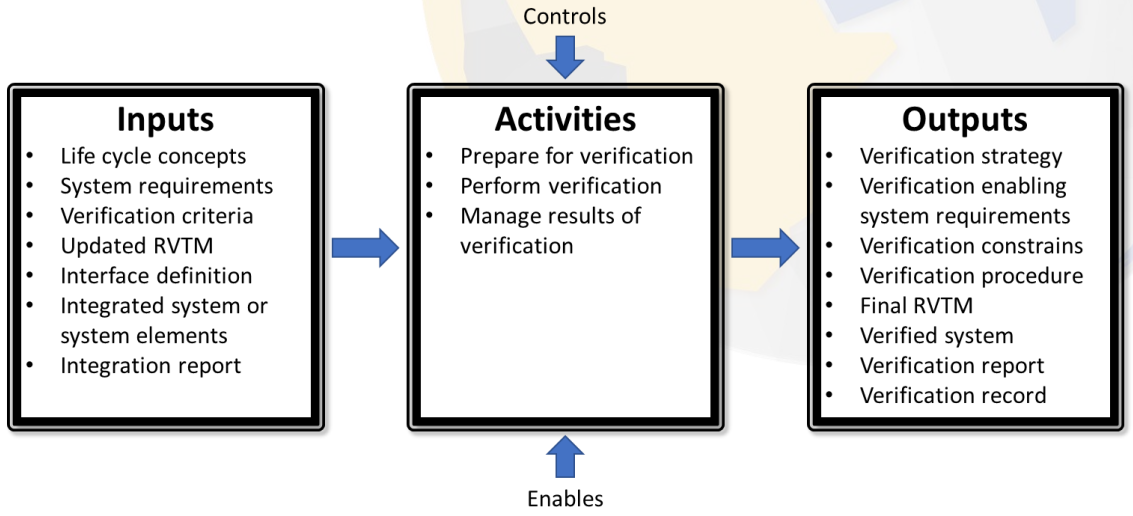
Outputs
- Verification strategy
- Verification enabling system requirements
- Verification constrains
- Verification procedure
- Final RVTM
- Verified system
- Verification report
- Verification record

Enables

- A process is best defined using inputs, outputs and activities to be developed in it.

- Based on the ISO 15288 Standard, a good implementation of the Verification Process must support the realization of the following activities:
  1. Prepare for verification
  2. Perform verification
  3. Manage results of verification

- Next Section: A detailed description on how to implement the activities using the V&V Studio



Verification Process : Activities

- 1- Prepare for verification.
  - Develop a strategy - that prioritizes the verification actions to minimize costs and risks while maximizing operational coverage of system behaviors
    - Determine the verification items
    - Establish verification constraints
    - Plan for the Verification Methods or techniques
    - Establish the scope of the Verification
  - Develop the verification procedures - that support the verification actions.
    - Schedule execution of VAs
    - Define the configuration of Submitted Items to Vas
  - Identify verification constraints on the system or system elements
    - arising from the verification strategy, that relate to specific system requirements, architecture elements, or design elements.
  - Ensure the necessary enabling systems, products, or services
    - required for the verification actions are available, when needed

Verification Process : Activities

- 2- Perform verification.
  - Implement the verification plan - That plan includes detailed descriptions for the selected verification actions:
    - Item to be verified
    - Expected results and success criteria
    - Selected verification method or technique
    - The data needed
    - The corresponding enabling systems, products, or services
  - Execute the Verification Actions and record the results.
    - Using the verification procedures,
  - Analyze the verification results
    - Against any established expectations and success criteria to determine whether the element being verified indicates conformance

Verification Process : Activities

- 3- Manage results of verification.
  - Identify and record verification results
    - and enter data in the Requirements Verification and Traceability Matrix (RVTM). Maintain the records per organizational policy.
  - Record anomalies
    - observed during the verification process and analyze and resolve the anomalies (corrective actions or improvements) using the quality assurance process.
  - Establish and maintain bidirectional traceability
    - of the verified system elements with the system architecture, design, and system and interface requirements that are needed for verification.
  - Provide baseline information for configuration management.
  - Update the verification strategy and schedule
    - according to the progress of the project; in particular, planned verification actions can be redefined or rescheduled as necessary.
  - Coordinate verification activities with the project manager
    - (e.g., for scheduling, acquisition of enablers, hiring of qualified personnel and resources), the architects or designers (e.g., for errors, defects, nonconformance reports), and the configuration manager (e.g., for versions of submitted items, requirements, architecture and design baselines, enablers, verification procedures).

- Common approaches and tips:
  - Beware the temptation to reduce the number of verification actions due to budget or schedule overruns.
  - In the progress of the project, it is important to know, at any time, what has not been verified in order to estimate the risks about possibly dropping out some verification actions.
  - Each system requirement should be quantitative, measurable, unambiguous, understandable, and testable. It is generally much easier and more cost-effective to ensure that requirements meet these criteria while they are being written. Requirements' adjustments made after implementation and/or integration are generally much more costly and may have wide-reaching redesign implications.
  - Avoid conducting verification only late in the schedule when there is less time to handle discrepancies.
  - Testing the actual system is expensive and is not the only verification technique. Other techniques such as simulation, analysis, review, etc. can be used on other engineering elements representing the SOI such as models, mock-ups, or partial prototypes.

Digitalizing the Verification Process

Using the V&V Studio

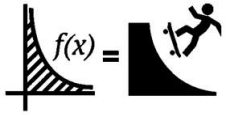
(following the ISO 15288)

Prepare for Verification

Select the Items to be Verified

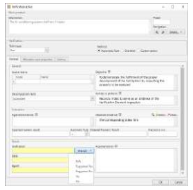
Define a Verification Action for each Verifiable Item

Prepare Resources of all types, Identify constraints, Enabling Systems, etc.



Define a Verification Technique for each Verifiable Item

Perform Verification



Execute the Verification Action for each Verifiable Item. If possible, the computer gathers the Information automatically

Computer applies the OK / KO decision process based on the standard guidelines.

Engineer defines the final state of the Verification process

Manage Results of Verification

Manage and record discovered anomalies and evidences

Track the Verification Process and manage Configuration

Build and maintain the RTVM

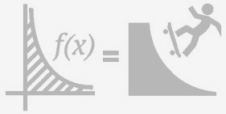
Provide proper reports

Prepare for Verification

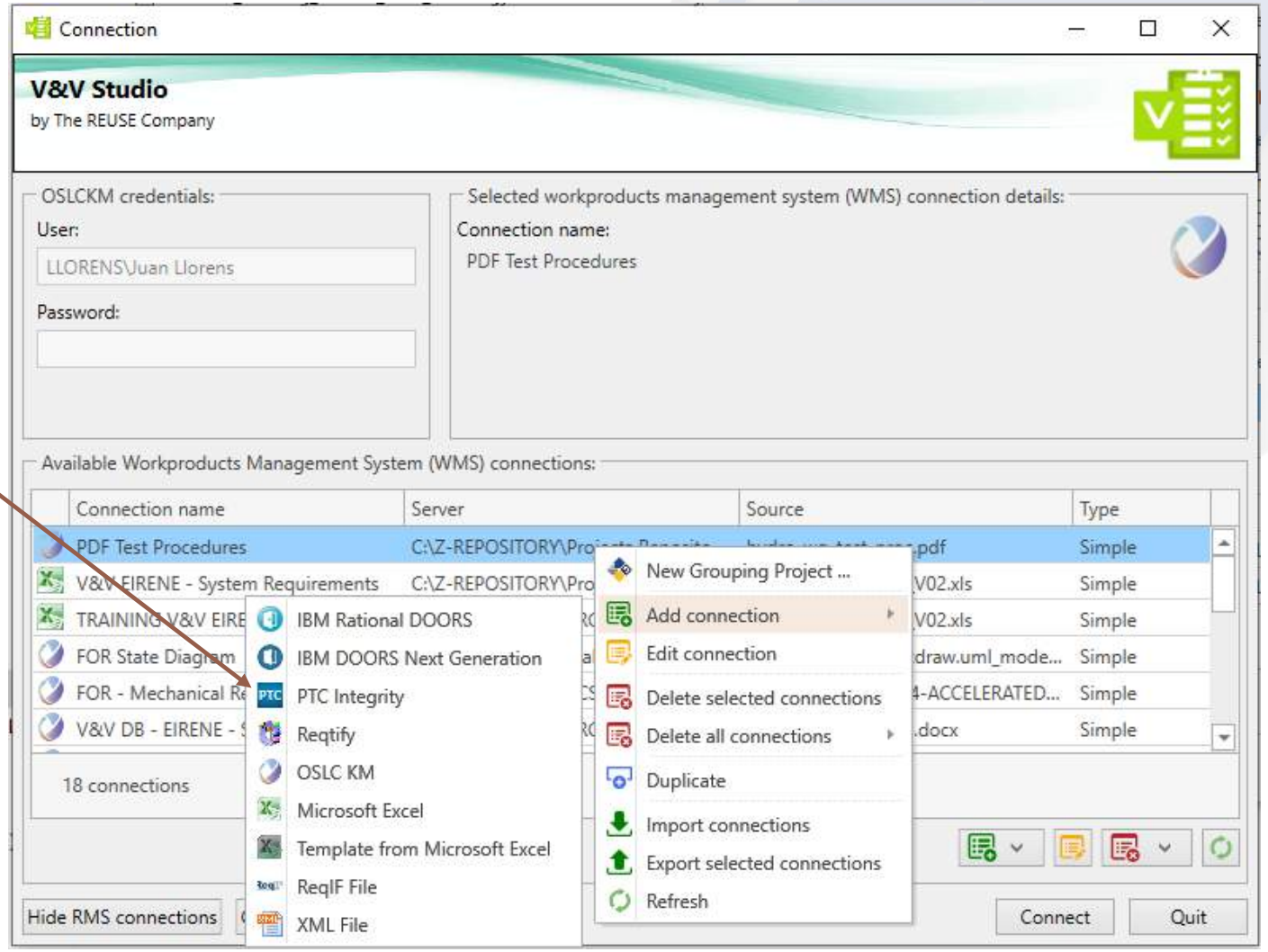
Select the Items to be Verified

Define a Verification Action for each Verifiable Item

Prepare Resources of all types, Identify constraints, Enabling Systems, etc.



Define a Verification Technique for each Verifiable Item



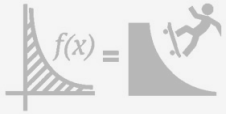
Verifiable Items and Source Items in the V&V Studio

Prepare for Verification

Select the Items to be Verified

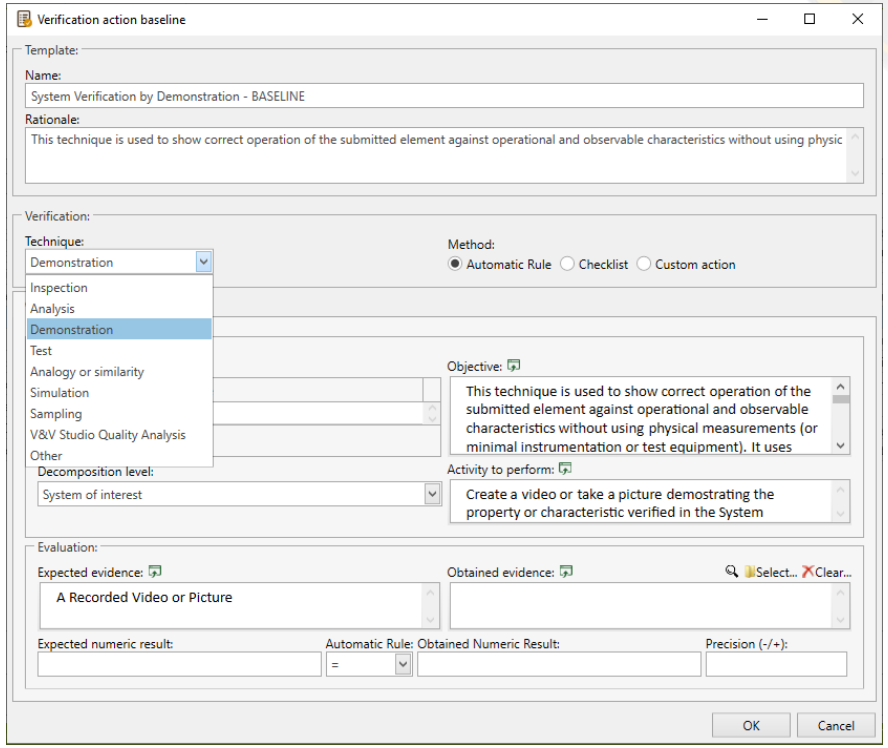
Define a Verification Action for each Verifiable Item

Prepare Resources of all types, Identify constraints, Enabling Systems, etc.



Define a Verification Technique for each Verifiable Item

By selecting a predefined VA template. i.e:
- Template for performing Inspection
- Template for producing a Check list
- Template for Simulation Analysis



Notion of VA Template

Verifiable Items and Source Items

Quality Project

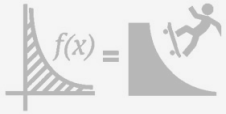
Define a Verification Strategy

Prepare for Verification

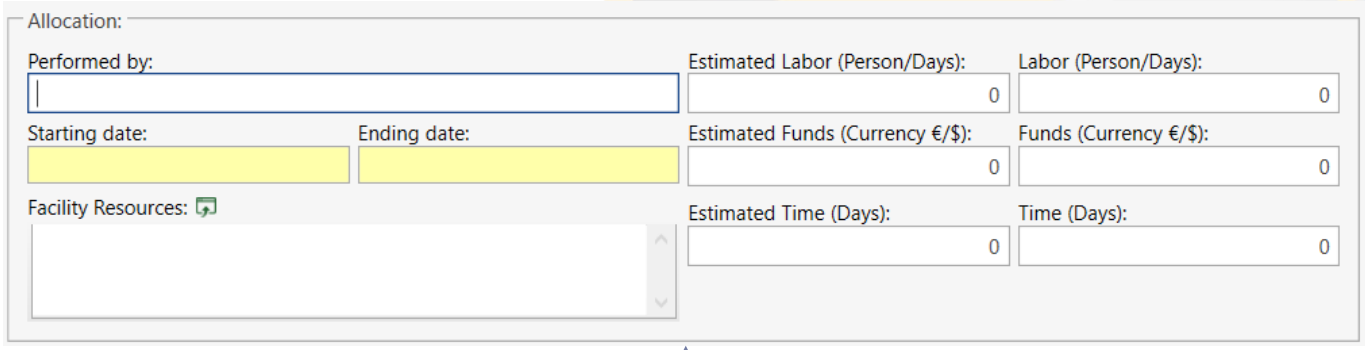
Select the Items to be Verified

Define a Verification Action for each Verifiable Item

Prepare Resources of all types, Identify constraints, Enabling Systems, etc.



Define a Verification Technique for each Verifiable Item

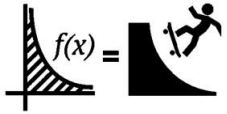


Prepare for Verification

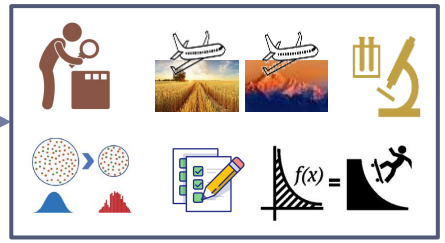
Select the Items to be Verified

Define a Verification Action for each Verifiable Item

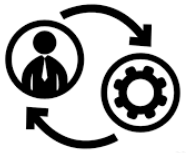
Prepare Resources of all types, Identify constraints, Enabling Systems, etc.



Define a Verification Technique for each Verifiable Item



Select one Verification Technique or define your own one



Define If the obtained results will be gathered manually or automatically

- manually: (A human engineer fills data in the VA manually

Defining customizable Check-lists

Defining values to be expected

- automatically (a **Calculation Function** gets the obtained data into the VA)

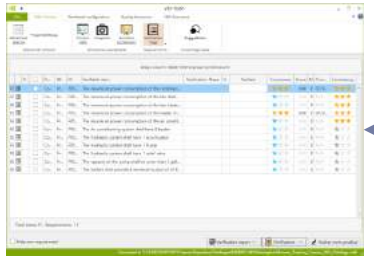
Connecting to other tools

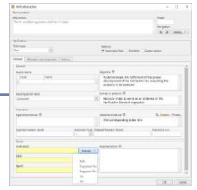
Calculating the Quality of Verifiable Item using RQA Tool

Defining your own Calculation Function

Perform Verification

Connect to the Source to collect the verifiable items





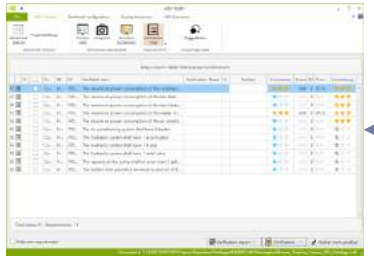
Execute the Verification Action for each Verifiable Item. If possible, the computer gathers the Information automatically

Computer applies the OK / KO decision process based on the standard guidelines.

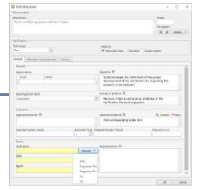
Engineer defines the final state of the Verification process

Perform Verification

Connect to the Source to collect the verifiable items



Engineer fills the VA information



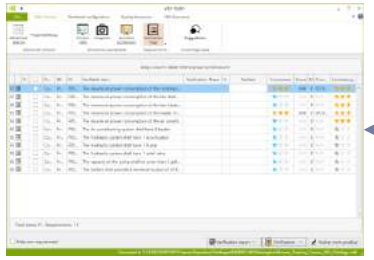
Execute the Verification Action for each Verifiable Item. If possible, the computer gathers the Information automatically

Computer applies the OK / KO decision process based on the standard guidelines.

Engineer defines the final state of the Verification process

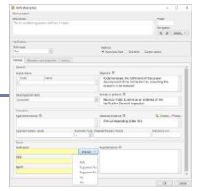
Perform Verification

Connect to the Source to collect the verifiable items



Engineer fills the VA information

Ask the computer to calculate the verification process (if automatic)



Execute the Verification Action for each Verifiable Item. If possible, the computer gathers the Information automatically

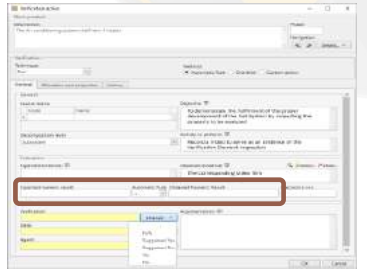
Computer applies the OK / KO decision process based on the standard guidelines.

Engineer defines the final state of the Verification process

Perform Verification

Execute the Verification Action for each Verifiable Item. If possible, the computer gathers the Information automatically

Computer applies the OK / KO decision process based on the standard guidelines.



V&V Studio
Systems Engineering Suite

Computer automatically compares expected results with obtained results
- Suggested Yes
- Suggested No
- NA

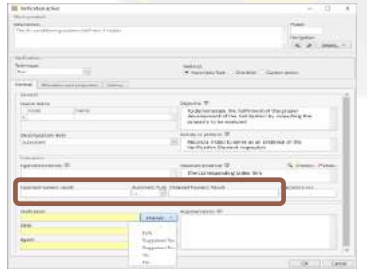
Engineer defines the final state of the Verification process

Perform Verification

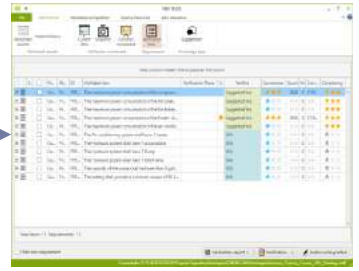
Execute the Verification Action for each Verifiable Item. If possible, the computer gathers the Information automatically

Computer applies the OK / KO decision process based on the standard guidelines.

Engineer defines the final state of the Verification process



Computer automatically compares expected results with obtained results
- Suggested Yes
- Suggested No
- NA



Full vision and management of the results is presented

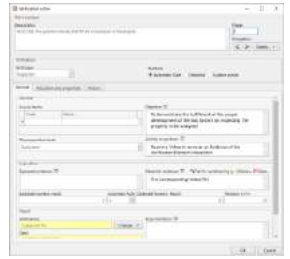
Perform Verification

Execute the Verification Action for each Verifiable Item. If possible, the computer gathers the Information automatically

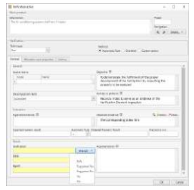
Computer applies the OK / KO decision process based on the standard guidelines.

Engineer defines the final state of the Verification process

→ The engineer fills the VA



Perform Verification



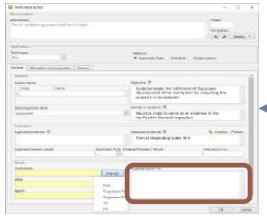
Execute the Verification Action for each Verifiable Item. If possible, the computer gathers the Information automatically

Computer applies the OK / KO decision process based on the standard guidelines.

Engineer defines the final state of the Verification process

A complete animated example for Quality Analysis Verification

The VA supports the reporting of anomalies



Manage Results of Verification

Manage and record discovered anomalies and evidences

Track the Verification Process and manage Configuration

Build and maintain the RTVM

Provide proper reports

Manage Results of Verification

Manage and record discovered anomalies and evidences

Manage Verification Snapshots or Verification evolution along time

Track the Verification Process and manage Configuration

Build and maintain the RTVM

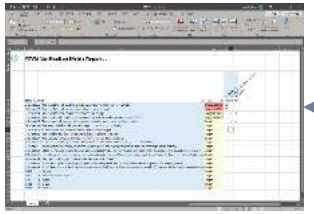
Provide proper reports

Manage Results of Verification

Manage and record discovered anomalies and evidences

Track the Verification Process and manage Configuration

A RTVM is created linking Verifiable Items and Source Items



Build and maintain the RTVM

Provide proper reports

Manage Results of Verification

Manage and record discovered anomalies and evidences

Track the Verification Process and manage Configuration

Build and maintain the RTVM

All reports can be produced in MS Word

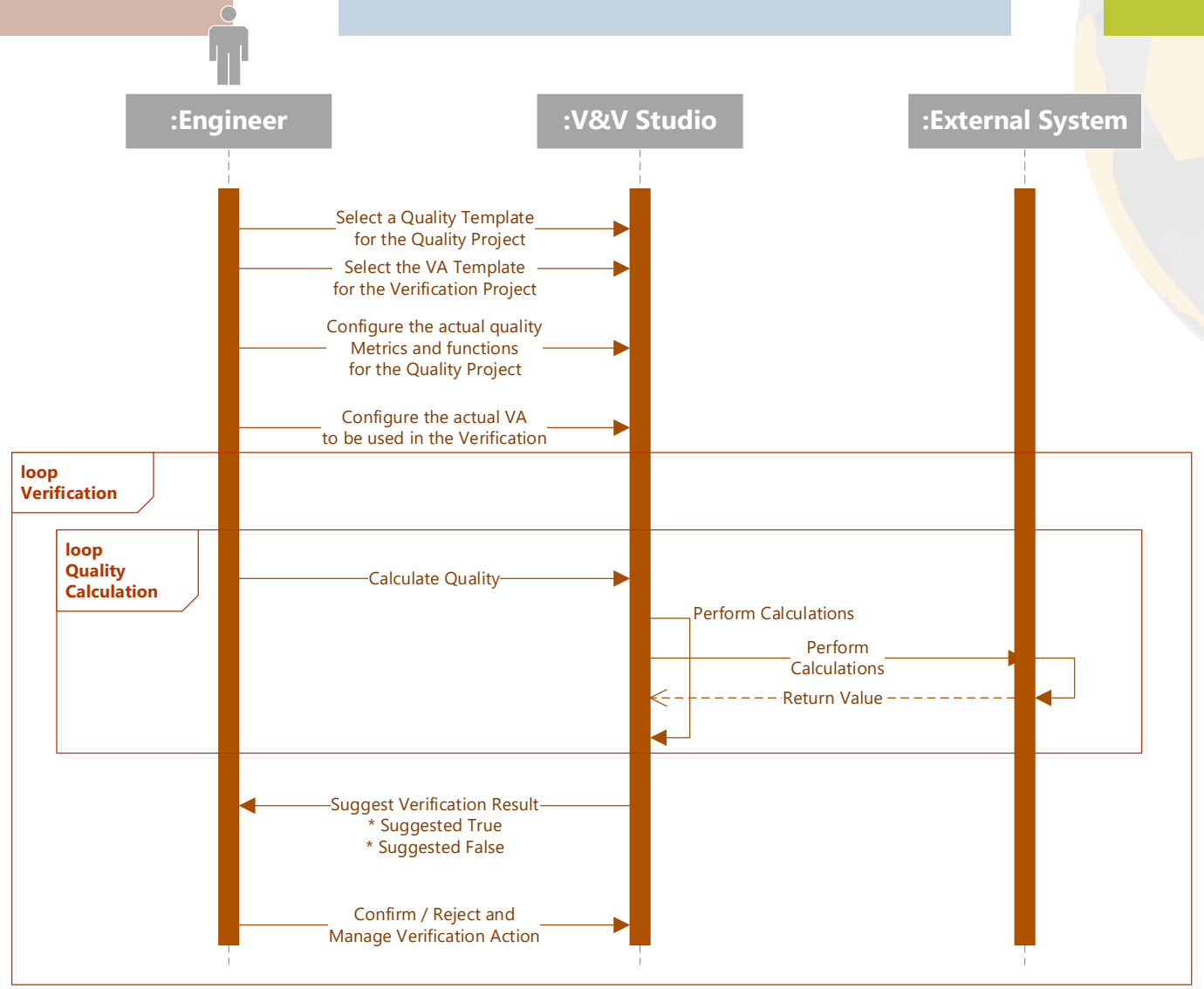
Provide proper reports

Verification Process summary for Quality calculation

Prepare for Verification

Perform Verification

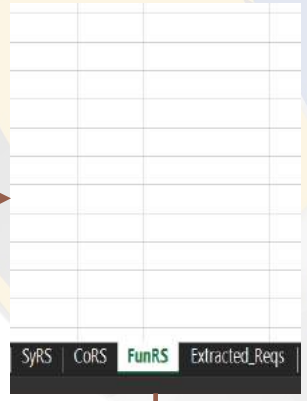
Manage Results of Verification



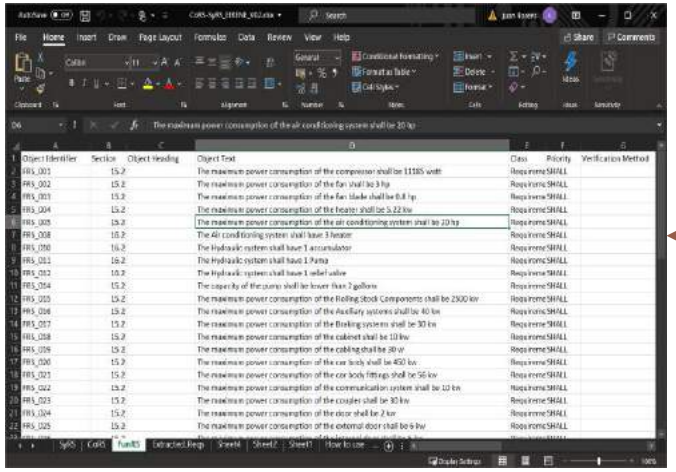
DEMO

Excel workbook as (project?)

(Excel sheets as (modules?)

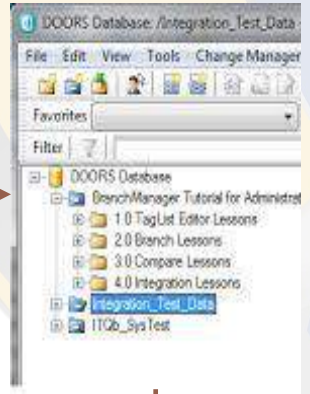


Excel rows as (work-products?)

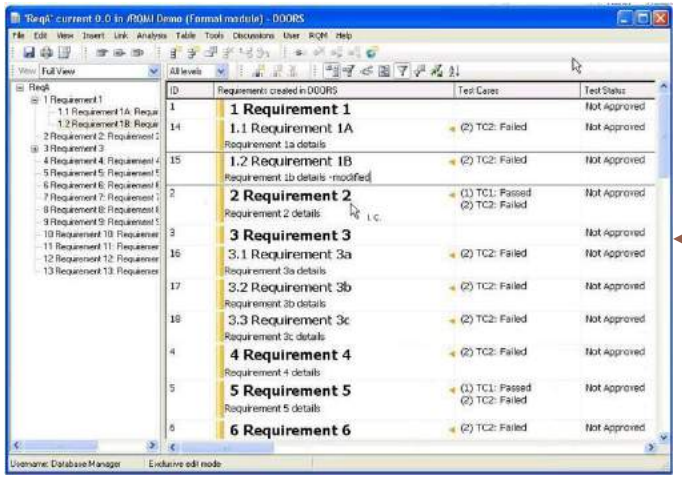


DOORS project from database as (project?)

DOORS modules as (modules?)

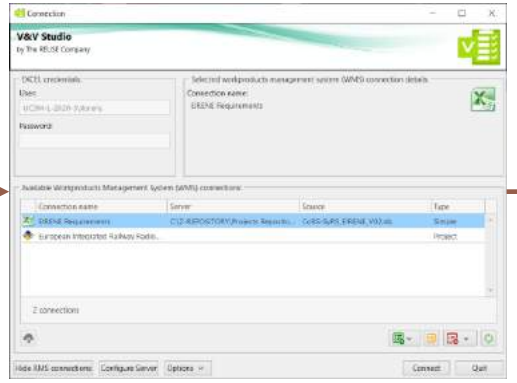


DOORS requirements as (work-products?)

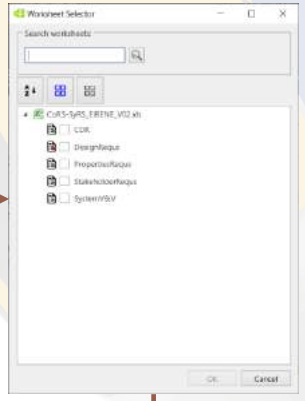


Start V&V Studio

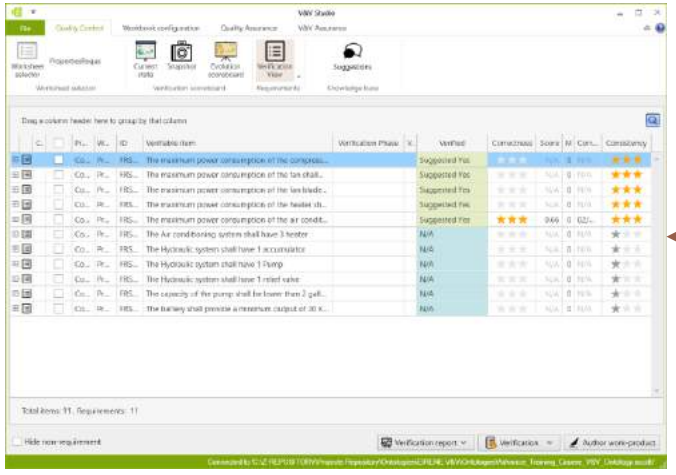
Select a connection to a source (project?)



(Optionally) select a (module?)



The Information is displayed in the screen (work-products?)



VV&V Studio: First time in the Tool – Main tabs

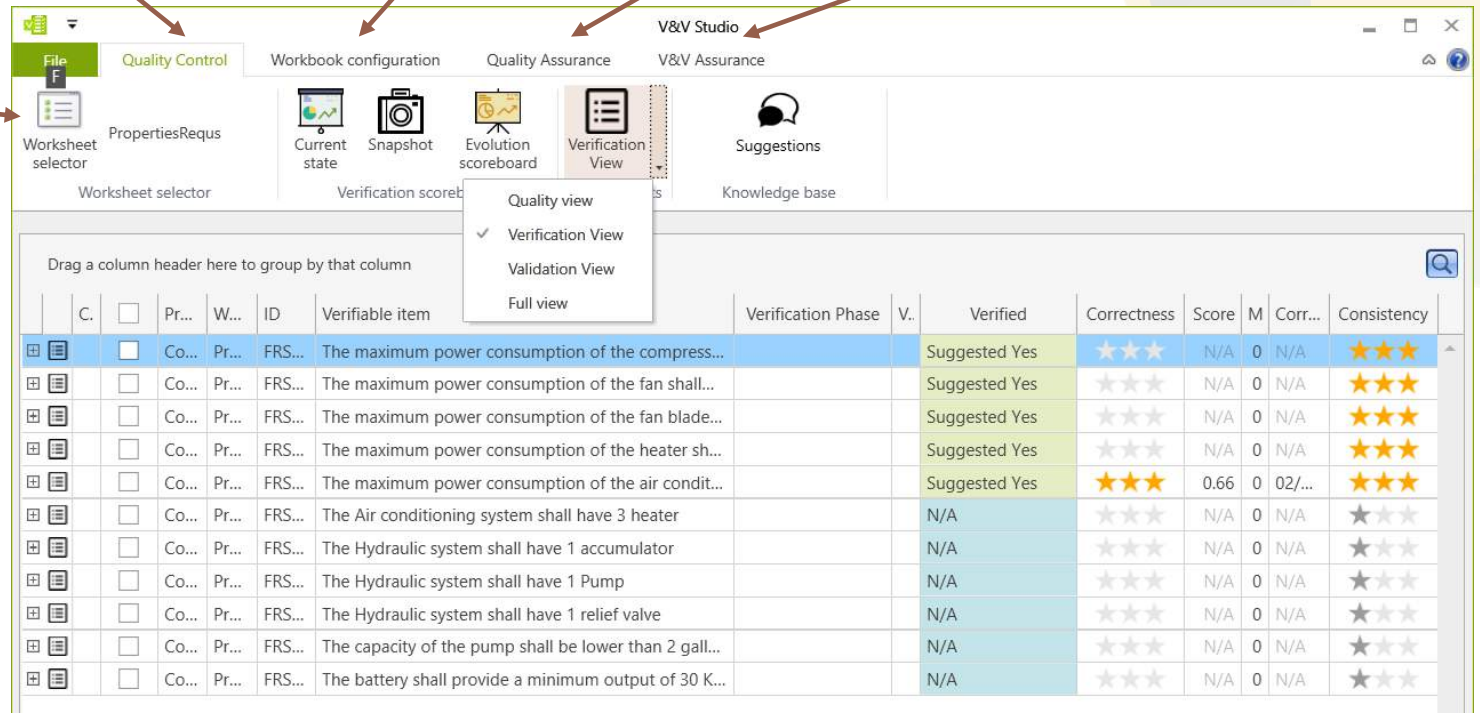
Assess Verification / Validation / Quality
For every single work-product

Configure Module
(called workbook)

Quality Assurance

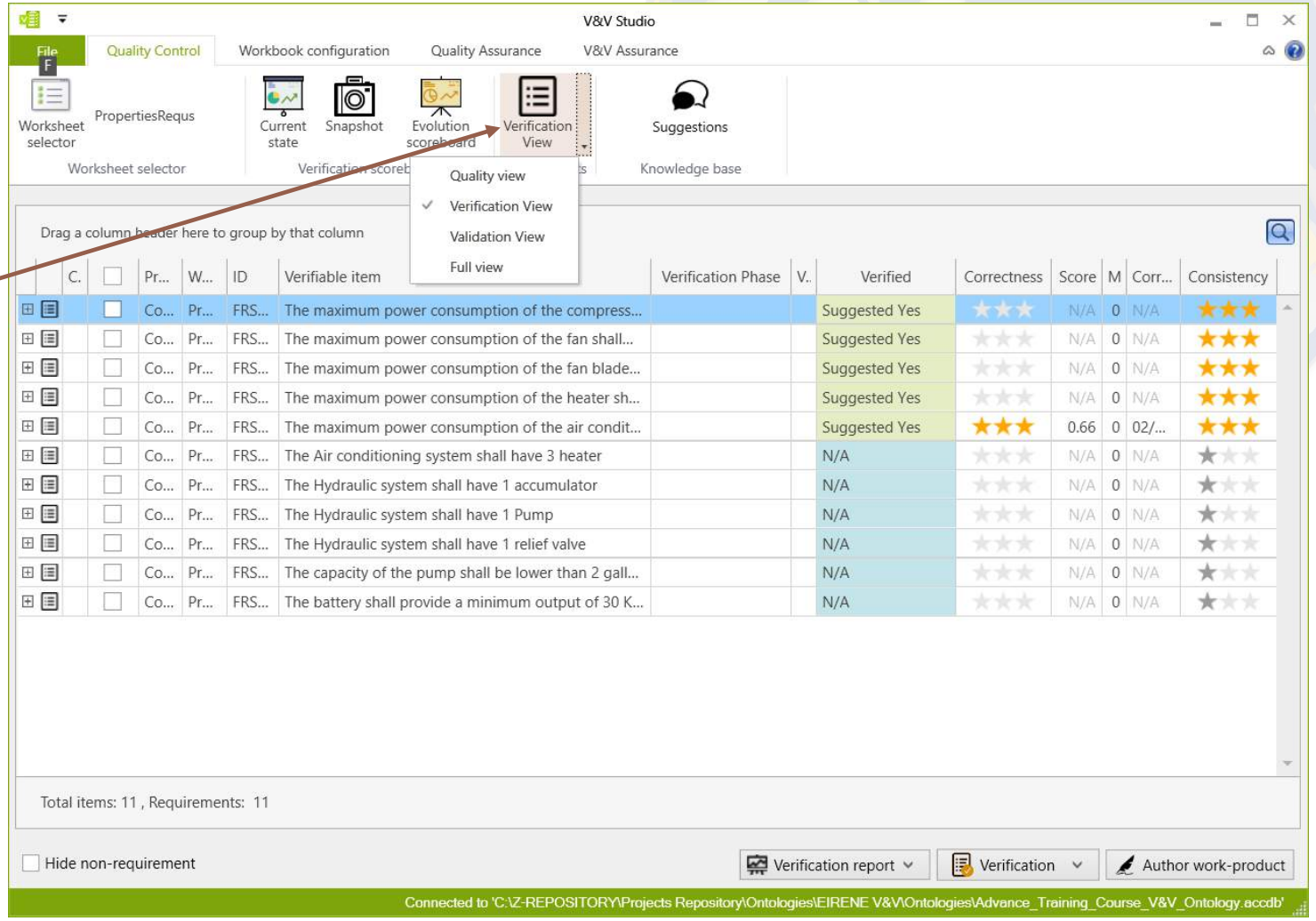
Verification / Validation
Assurance

Module
Selection

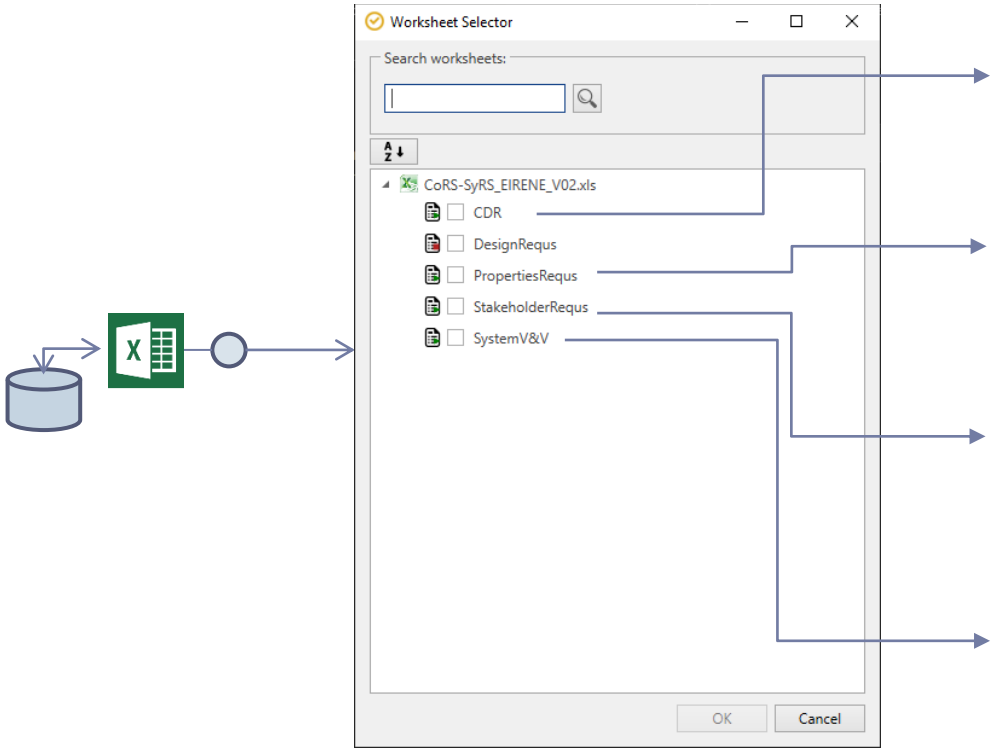


Switching Verification and Validation Mode

- In Quality Control tab (Modified in V20)
- Select the desired view and the tool is reconfigured
  - Obs.. It is possible to work as
    - Verification
    - Validation
    - Quality !!!



DEMO Description



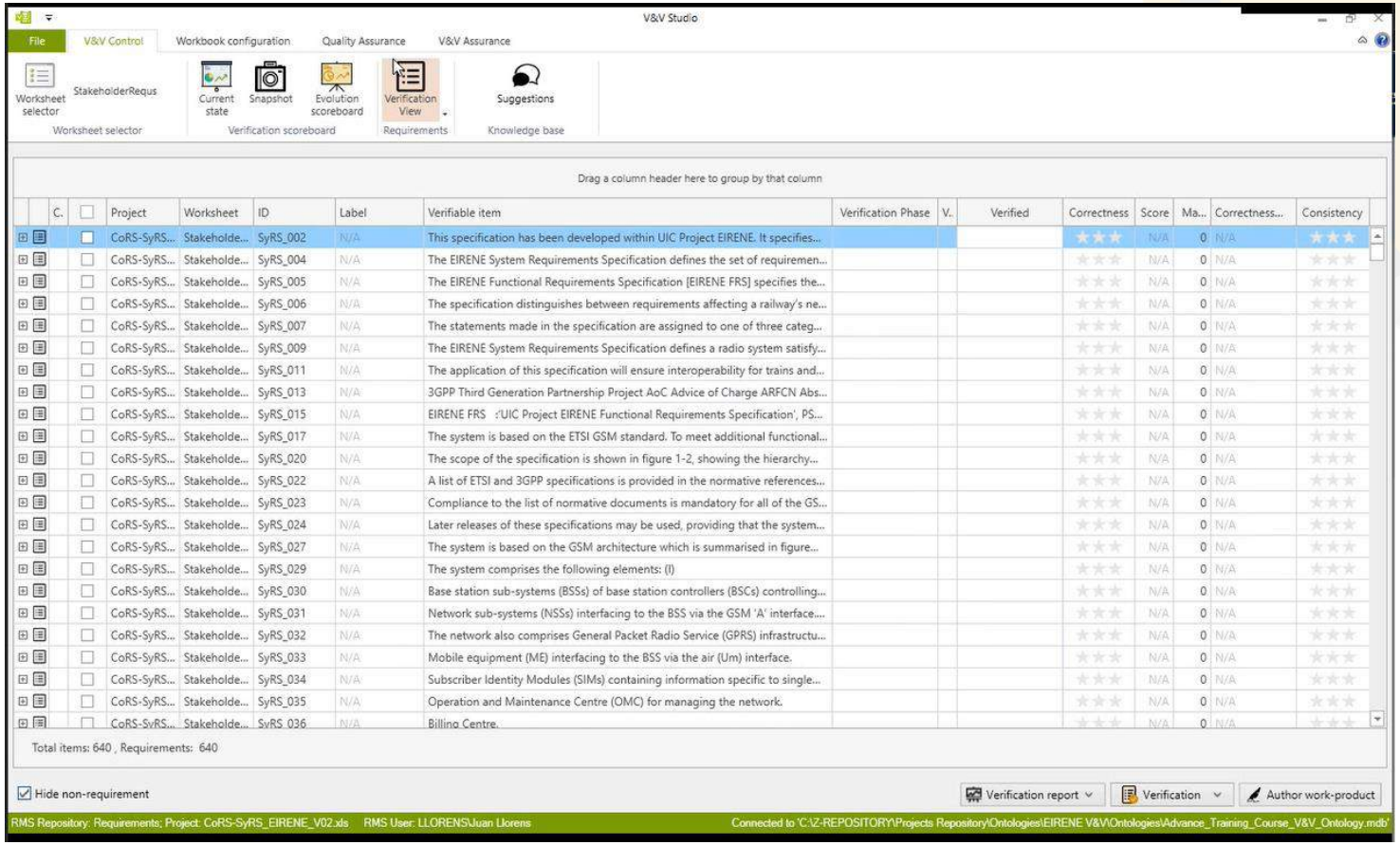
Critical Design Review Verification → Using a Check List from CMMI guidelines and Raytheon Systems Engineering practice

Property Requirements → Using a Consistency Quality Analysis Metric model

Stakeholder Requirements → Using a Correctness Quality Analysis Metric model

Verification of the System → Using a simulation model by running a FMU

DEMO




Q&A

contact@reusecompany.com